

What is Claimed is:

1. A circuit that corrects errors in configuration data stored on a programmable logic device comprising:

5 a memory in which the configuration data and error check data associated with the configuration data is stored; and

error correction circuitry coupled to at least some of the memory to analyze the configuration data stored in the memory to determine if any values
10 have changed after initial configuration of the memory and to correct any values that have changed.

2. The circuit of claim 1 wherein the error correction circuitry comprises at least one scrubbing circuit operative to:

5 read from the memory a portion of the configuration data and an associated portion of the error check data;

apply an error correcting code on the portion of the configuration data and the associated portion of the error check data to determine whether at
10 least one bit in the portion of the configuration data has an error and to correct the at least one bit that has the error; and

write into the memory the at least one corrected bit.

3. The circuit of claim 2 wherein the scrubbing circuit is associated with a subset of the configuration data and an associated subset of the error check data.

4. The circuit of claim 1 wherein:

the configuration data is stored in an array of representative rows and representative columns of cells, each cell storing one bit of the configuration data; and

the error check data is stored in a last representative column of cells and a last representative row of cells in the array, each cell storing one bit of the error check data.

5. The circuit of claim 4 wherein the error correction circuitry comprises:

first circuitry having an input operative to receive data from each cell in a representative row of the array and an output, the first circuitry generating a first parity for the data in the representative row at the output;

second circuitry having an input operative to receive data from each cell in a representative column of the array and an output, the second circuitry generating a second parity for the data in the representative column at the output;

third circuitry having a first input operative to receive the output of the first circuitry, having a second input operative to receive the output of the second circuitry, and an output, the third circuitry sending a signal at the output indicative of whether an error has occurred in a cell in the representative row and the representative column based on the first parity and the second parity; and

fourth circuitry having a first input operative to receive the output of the third circuitry, a second input operative to receive data from the cell

in the representative row and the representative
25 column, and an output, the fourth circuitry sending a
signal at the output having a correct value.

6. The circuit of claim 5 wherein the
correct value is:

the data from the cell when the output
of the first logic gate indicates that no error has
5 occurred; and

the complement of the data from the cell
when the output of the first logic gate indicates that
the error has occurred.

7. The circuit of claim 5 further
comprising fifth circuitry operative to write the
correct value into the cell.

8. The circuit of claim 4 wherein the error
correction circuitry comprises:

first circuitry having an input
operative to receive data from all but one cell in a
5 representative row of the array and an output, the
first circuitry generating a first parity for the data
from all but the one cell in the representative row at
the output;

second circuitry having an input
10 operative to receive data from all but the one cell in
a representative column of the array and an output, the
second circuitry generating a second parity for the
data from all but the one cell in the representative
column at the output; and

15 third circuitry having a first input
operative to receive the output of the first circuitry,
a second input operative to receive the output of the

second circuitry, a third input operative to receive
data from the one cell, and an output, the third
20 circuitry generating a correct value at the output.

9. The circuit of claim 8 further
comprising fourth circuitry operative to write the
correct value into the one cell.

10. The circuit of claim 1 wherein each bit
of the configuration data is stored in a first cell, a
second cell, and a third cell in the memory.

11. The circuit of claim 10 wherein the
error correction circuitry generates as output a same
bit value that is stored in at least two of the first
cell, the second cell, and the third cell.

12. The circuit of claim 11 wherein the
error correction circuitry comprises circuitry having a
first input operative to receive a bit from the first
cell, a second input operative to receive a bit from
5 the second cell, a third input operative to receive a
bit from the third cell, and an output, the circuitry
generating a correct bit value at the output.

13. The circuit of claim 12 further
comprising second circuitry operative to write the
correct bit value into at least one of the first cell,
the second cell, and the third cell.

14. The circuit of claim 1 further
comprising:

a resistive element coupled to an output
of the error correction circuitry; and

5 a capacitive load coupled to the

resistive element, wherein the resistive element and the capacitive load are operative to reduce static hazards associated with the error correction circuitry.

15. The circuit of claim 14 wherein the resistive element is one of a polysilicon wire, a current starved pass gate, and a current starved inverter.

16. A digital processing system comprising:
processing circuitry;
a memory coupled to the processing circuitry; and
5 a programmable logic device as defined in claim 1 coupled to the processing circuitry and the memory.

17. A printed circuit board on which is mounted a programmable logic device as defined in claim 16.

18. The printed circuit board defined in claim 17 further comprising:
a memory mounted on the printed circuit board and coupled to the programmable logic device.

19. The printed circuit board defined in claim 17 further comprising:
processing circuitry mounted on the printed circuit board and coupled to the programmable
5 logic device.

20. A circuit that corrects errors in configuration data stored on a programmable logic device comprising:

5 a memory in which the configuration data
and error check data associated with the configuration
data are stored; and

at least one scrubber coupled to the
memory and operative to:

10 read from the memory a portion of
the configuration data and an associated portion of the
error check data,

apply an error correcting code on
the portion of the configuration data and the portion
of the error check data to determine whether at least
15 one bit in the portion of the configuration data has an
error and to correct the at least one bit that has the
error, and

write into the memory the at least
one corrected data bit.

21. The circuit of claim 20 further
comprising one scrubber associated with the
configuration data and the error check data.

22. The circuit of claim 20 further
comprising more than one scrubber each associated with
a subset of the configuration data and an associated
subset of the error check data.

23. The circuit of claim 20 wherein the
error correcting code is one of a Hamming Code, a Reed-
Solomon Code, and a Product Code.

24. A circuit that corrects errors in
configuration data stored on a programmable logic
device comprising:

5 a memory array of representative rows
and representative columns of cells in which the

configuration data and error check data associated with the configuration data are stored;

first circuitry having an input operative to receive data from each cell in a representative row of the array and an output, the
10 first circuitry generating a first parity for the data in the representative row at the output;

second circuitry having an input operative to receive data from each cell in a representative column of the array and an output, the
15 second circuitry generating a second parity for the data in the representative column at the output;

third circuitry having a first input operative to receive the output of the first circuitry, having a second input operative to receive the output of the second circuitry, and an output, the third
20 circuitry sending a signal at the output indicative of whether an error has occurred in a cell in the representative row and the representative column based on the first parity and the second parity; and
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fourth circuitry having a first input operative to receive the output of the third circuitry, a second input operative to receive data from the cell in the representative row and the representative
30 column, and an output, the fourth circuitry sending a signal at the output having a correct value.

25. The circuit of claim 24 wherein the correct value is:

the data from the cell when the output of the first logic gate indicates that no error has
5 occurred; and

the complement of the data from the cell

when the output of the first logic gate indicates that an error has occurred.

26. The circuit of claim 24 further comprising fifth circuitry operative to write the correct value into the cell.

27. A circuit that corrects errors in configuration data stored on a programmable logic device comprising:

5 a memory array of representative rows and representative columns of cells in which the configuration data and error check data associated with the configuration data are stored;

10 first circuitry having an input operative to receive data from all but one cell in a representative row of the array and an output, the first circuitry generating a first parity for the data from all but the one cell in the representative row at the output;

15 second circuitry having an input operative to receive data from all but the one cell in a representative column of the array and an output, the second circuitry generating a second parity for the data from all but the one cell in the representative column at the output; and

20 third circuitry having a first input operative to receive the output of the first circuitry, a second input operative to receive the output of the second circuitry, a third input operative to receive data from the one cell, and an output, the third
25 circuitry generating a correct value at the output.

28. The circuit of claim 27 further comprising fourth circuitry operative to write the correct value into the one cell.

29. A circuit that corrects errors in configuration data stored on a programmable logic device comprising:

5 a first memory cell in which a configuration bit from the configuration data is stored;

a second memory cell in which the configuration bit is stored;

10 a third memory cell in which the configuration bit is stored; and

circuitry having a first input operative to receive a bit value from the first memory cell, a second input operative to receive a bit value from the second memory cell, a third input operative to receive a bit value from the third memory cell, and an output, the circuitry generating as the output a correct bit value that is stored in at least two of the first memory cell, the second memory cell, and the third memory cell.

30. The circuit of claim 29 further comprising second circuitry operative to write the correct bit value into at least one of the first memory cell, the second memory cell, and the third memory cell.

31. A circuit that corrects errors in data stored in an embedded memory block on a programmable logic device comprising:

an embedded memory array in which the

5 data is stored; and

error correction circuitry coupled to
the embedded memory array to analyze the data stored in
the embedded memory array to determine if any values
have changed and to correct any values that have
10 changed.

32. The circuit of claim 31 wherein, during
a write operation, the error correction circuitry
computes error check bits associated with the data.

33. The circuit of claim 32 wherein the
error check bits are stored in the embedded memory
array.

34. The circuit of claim 32 wherein, during
a read operation, the error correction circuitry:

reads the data and the error check bits
from the embedded memory array;

5 performs an error correcting code on the
data and the error check bits to determine whether an
error has occurred in the data; and

corrects the data if the error has
occurred.

35. The circuit of claim 31 wherein the
error correction circuitry is implemented in hardware
in the embedded memory block.

36. The circuit of claim 31 wherein the
error correction circuitry is implemented in soft logic
on the programmable logic device.

37. A method for correcting errors in
configuration data stored on a programmable logic

device comprising:

generating and storing error check data
5 associated with the configuration data in a memory;
reading a portion of the configuration
data and an associated portion of the error check data;
determining if an error has occurred
based on the portion of the configuration data and the
10 associated portion of the error check data; and
correcting the portion of the
configuration data in response to the determining.

38. The method of claim 37 wherein the
portion of the configuration data is at least one
representative column of cells in the memory.

39. The method of claim 37 wherein the
portion of the configuration data is at least one
partial representative column of cells in the memory.

40. The method of claim 37 wherein the
portion of the configuration data is at least two
partial representative columns of cells in the memory
that are physically contiguous.

41. The method of claim 37 wherein the
portion of the configuration data is at least two
partial representative columns of cells in the memory
that are physically non-contiguous.

42. The method of claim 37 wherein the
determining comprises applying an error correcting code
on the portion of the configuration data and the
associated portion of the error check data.

43. The method of claim 42 wherein the error correcting code is one of a Hamming Code, a Reed-Solomon Code, and a Product Code.

44. The method of claim 37 wherein the correcting comprises writing the corrected portion of the configuration data into the memory.

45. A method for correcting errors in configuration data stored on a programmable logic device comprising:

generating and storing a parity bit
5 associated with each representative row and each
representative column of memory cells in which the
configuration data is stored;
computing a first parity on a given
representative row of memory cells;
10 computing a second parity on a given
representative column of memory cells;
determining if an error has occurred in
a cell in the given representative row and the given
representative column based on the first parity and the
15 second parity; and
correcting the data in the cell in
response to the determining.

46. The method of claim 45 wherein the
parity bit associated with each representative row and
each representative column is a logic value that allows
the associated representative row or representative
5 column to have one of even parity and odd parity.

47. The method of claim 45 wherein correcting the data comprises inverting the logic of the data in the cell for output.

48. The method of claim 45 wherein correcting the data comprises writing the corrected data into the cell.

49. A method for correcting errors in configuration data stored on a programmable logic device comprising:

generating and storing a parity bit
5 associated with each representative row and each representative column of memory cells in which the configuration data is stored;

computing a first parity on all but one cell in a given representative row of memory cells;

10 computing a second parity on all but the one cell in a given representative column of memory cells; and

generating a correct value for the data in the one cell based on the first parity, the second
15 parity, and data in the one cell.

50. The method of claim 49 wherein the parity bit associated with each representative row and each representative column is a logic value that allows the associated representative row or representative
5 column to have one of even parity and odd parity.

51. The method of claim 49 further comprising writing the corrected data into the one cell.

52. A method for correcting errors in configuration data stored on a programmable logic device comprising:

5 storing a same configuration bit from the configuration data into a first memory cell, a second memory cell, and a third memory cell;

determining what same bit value is stored in at least two of the first memory cell, the second memory cell, and the third memory cell; and

10 sending as output a correct bit value in response to the determining.

53. The method of claim 52 further comprising writing the same bit value in at least one of the first memory cell, the second memory cell, and the third memory cell.